CET2113C – Advanced Digital Circuits

Lab 4 – VHDL Multiplexers, Comparators, and Tri-State Buffers

Objective

The objective of this lab is to implement, in VHDL, all of the Standard combinational circuits we will be using to implement a simple Microprocessor. These include an ALU, Multiplexer, Comparator, Tri-State Buffer.

Part II: Multiplexer

Using the Multiplexer design from ch 4, design an 8-to-1, 8-bit wide multiplexer. Create a simulation for the Multiplexer, and show the simulation result to Dr. Poe for credit. ***NOTE THIS IS NOT EXACTLY THE SAME AS THE BOOK EXAMPLE.***

Part III: Comparators

Using the Comparator design from ch 4, design an 8 bit comparator that tests, x=y, x>y, x<y. Create a simulation for the Comparators, and show the simulation result to Dr. Poe for credit. ***NOTE THIS IS NOT EXACTLY THE SAME AS THE BOOK EXAMPLE.***

Part IV: Tri-State Buffer.

Using the Tri-State Buffer design from ch 4, design a 16 bit wide tri-state buffer. Create a simulation for the Tri-State Buffer, and show the simulation result to Dr. Poe for credit. ***NOTE THIS IS NOT EXACTLY THE SAME AS THE BOOK EXAMPLE.***